Digital Filters for Digital Phase-Locked Loops

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An s/z hybrid model for a general phase-locked loop is proposed in this article. The impact of the loop filter on the stability, gain margin, noise-equivalent bandwidth, steady-state error and time response is investigated. A specific digital filter is selected which maximizes the overall gain margin of the loop. This filter can have any desired number of integrators. Three integrators are sufficient in order to track a phase jerk with zero steady-state error at loop update instants. This filter has one zero near z = 1.0 for each integrator. The total number of poles of the filter is equal to the number of integrators plus two.

I. Introduction

In this article, the impact of a general digital filter on the gain margin, noise-bandwidth, steady-state error and transient response of a digital phase-locked loop is investigated. For the proposed s/z-domain model of a digital phase-locked loop, a wide variety of digital filters was investigated by analysis and by simulation.

A specific type of filter is suggested which has the property of having one zero for each filter integrator. The total number of poles of this filter equals the number of integrators (poles at $z = 1$) plus two. All loop poles are forced to remain on or near the real axis for the maximum possible range of loop gain. The loop remains stable with any number of integrators. The noise bandwidth increases slightly with the number of integrators. Gain margin and transient response are almost insensitive to the number of integrators.

The proposed type of filter allows tracking very high Doppler rates with zero steady-state error (at loop update instants).

II. Loop Components

The basic components of our digital loop (see Fig. 1) are: (a) an integrate-and-dump circuit, which also serves as an analog-to-digital converter, (b) a digitally controlled oscillator (DCO), which also serves as a digital-to-analog converter, and (c) a loop filter. These components are modeled in the hybrid s/z domain as follows:

(a) Integrate-and-dump (According to Ref. 1):

$$I(s, z) = \frac{\epsilon(z)}{\phi(s)} = G_Q \frac{1}{s} \frac{z - 1}{z} \tag{1}$$

(b) DCO[1]:

$$D(s, z) = \frac{\hat{\theta}(s)}{\hat{\theta}_d(z)} = \frac{1 - \exp(-sT)}{s^2} = \frac{1 - z^{-1}}{s^2} \quad (2)$$

(c) Loop Filter:

$$F(z) = \frac{\hat{\dot{\theta}}(z)}{\epsilon(z)} = K_f \frac{(1 - z_1 z^{-1})(1 - z_2 z^{-1}) \ldots (1 - z_m z^{-1})}{(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} \quad (3)$$

where

G_Q represents the combined gain of the phase detectors, and other loop components and is proportional to the power of the input signal.

T is the loop update time

$\{z_i\}$ are the zeros of the loop filter

$\{p_i\}$ are the poles of the loop filter

In the actual implementation of the loop filter, there is a time delay between the instants the error signal ϵ_i is read and the estimated phase rate $\hat{\dot{\theta}}_i$ is computed. This time delay is modeled as

$$T_d(s) = \frac{\hat{\dot{\theta}}_d(z)}{\hat{\dot{\theta}}(z)} = \exp(-sgT) \quad (4)$$

where $0 < g < 1.0$ is the normalized time delay

$$g = \frac{T_c}{T} \quad (5)$$

The term T_c is the computation time, and $\hat{\dot{\theta}}_d(z)$ is $\hat{\dot{\theta}}(z)$ delayed by T_c seconds.

Referring to Fig. 1, we see that

$$X(s) = \frac{\phi(s)}{s} = \frac{\theta(s)}{s} - \hat{\dot{\theta}}(z)[1 - \exp(-sT)] \frac{\exp(-sgT)}{s^3} \quad (6)$$

[1]The DCO can be modeled as a Digital-to-Analog converter for which the transfer function is

$$\frac{\hat{\theta}(s)}{\hat{\dot{\theta}}_d(z)} = \frac{1 - \exp(-sT)}{s}$$

Multiplying this by $1/s$ converts $\hat{\dot{\theta}}(s)$ to $\hat{\theta}(s)$.

Taking the z transform of Eq. (6), we obtain[2]

$$X(z) = \left(\frac{\phi(s)}{s}\right)^* = \left(\frac{\theta(s)}{s}\right)^* - \frac{T^2}{2} \frac{[(1-g)^2 z^2 + (1 + 2g - 2g^2) z + g^2)]}{z(z-1)^2} \hat{\dot{\theta}}(z) \quad (7)$$

where the asterisk denotes the z transform of the expression inside the parentheses. Equation (7) has the block diagram representation of Fig. 2. Using the above equation, together with Eqs. (1) and (3), the open-loop transfer function is

$$G(z) \triangleq \left(\frac{\hat{\theta}(s)}{s}\right)^* \frac{1}{\left(\frac{\phi(s)}{s}\right)^*} = \frac{\hat{\theta}_1(z)}{X(z)}$$

$$= G \frac{(z^2 + C_1 z + C_2)}{z^2(z-1)} F(z) \quad (8)$$

where

$$G = \frac{G_Q T^2}{2} (1-g)^2 \quad (9)$$

is the effective loop gain

$$C_1 = (1 + 2g - 2g^2)/(1-g)^2 \quad (10)$$

$$C_2 = g^2/(1-g)^2 \quad (11)$$

Using Eq. (8), the closed-loop transfer function will be

$$H(z) \triangleq \frac{\hat{\theta}_1(z)}{(\theta(s)/s)^*} = \frac{G(z)}{1 + G(z)} \quad (12)$$

III. Selection of the Loop Filter

In general, a digital filter can be expressed by the following difference equation:

$$\hat{\dot{\theta}}_i = \sum_{j=1}^{n} \alpha_j \hat{\dot{\theta}}_{i-j} + \sum_{j=0}^{m} \beta_j \epsilon_{i-j} \quad (13)$$

[2]In general, given a function $L(s)$, we always have

$$[\exp(-sgT) L(s)]^* \triangleq L(z, m), \quad m = 1 - g$$

where $L(z, m)$ is the modified z transform of $L(s)$. This technique is used to obtain Eq. (7) from Eq. (6).

The direct form I realization of this filter is shown in Fig. 3. Figure 4 depicts the same filter in the direct form II realization. The transfer function corresponding to Eq. (13) is

$$F(z) = \frac{\hat{\theta}(z)}{\epsilon(z)} = \frac{\beta_0 + \beta_1 z^{-1} + \beta_2 z^{-2} + \ldots \beta_m z^{-m}}{1 - \alpha_1 z^{-1} - \alpha_2 z^{-2} \ldots \alpha_n z^{-n}} \quad (14)$$

which can be factored into the pole-zero representation of Eq. (3).

With $\beta_0 = 1$ and $m < n$, Eq. (14) can be rewritten as follows:

$$F(z) = \frac{\left(z^m + \beta_1 z^{m-1} + \ldots \beta_m\right) z^{n-m}}{z^n - \alpha_1 z^{n-1} - \ldots - \alpha_n} \quad (15)$$

$$= \frac{(z - z_1)(z - z_2) \ldots (z - z_m) z^{n-m}}{(z - p_1)(z - p_2) \ldots (z - p_n)} \quad (16)$$

This filter will always have n poles and n zeros, such that $n - m$ of the zeros will be at $z = 0$.

The filter controls the following four main parameters of the phase-locked loop:

(1) Gain margin

(2) Noise-equivalent bandwidth

(3) Steady-state error

(4) Transient response

The selection of proper values for z_i and p_i is dictated by the necessity of optimizing the above loop parameters. In what follows, we will address each optimization criterion individually.

A. Stability and Gain Margin

Inserting Eq. (16) in Eq. (8) and using Eq. (12), the closed loop transfer function with an n^{th} order filter is

$$H(z) = \frac{G(z - z_a)(z - z_b)(z - z_1)(z - z_2) \ldots (z - z_m) z^{n-m} \ldots}{z^2(z - 1)(z - p_1)(z - p_2) \ldots (z - p_n)}$$

$$\frac{}{+ G(z - z_a)(z - z_b)(z - z_1)(z - z_2) \ldots (z - z_m) z^{n-m}} \quad (17)$$

Here z_a and z_b are the roots of $(z^2 + C_1 z + C_2)$ in Eq. (8). These two zeros result from nonzero computation time. For example, assuming that $g = 0.5$ (a computation time of half an update time), then $z_a = -0.1716$ and $z_b = -5.8283$.

For the effective loop gain G changing from $G = 0$ to $G = \infty$, the poles of $H(z)$ will move starting at the location of the open-loop poles, p_i, of $G(z)$ and ending at the location of the open-loop zeros, z_i, of $G(z)$. The loop will be stable when *all* the poles of $H(z)$ are inside the unit circle in the complex z-plane. Thus, in order to increase the gain margin, given that other constraints are met, we want to place all z_i's and p_i's such that the range of G that maintains a stable loop is maximum.

In order to track high Doppler rates with zero or minimum steady-state error, the loop should have 2 or more integrators, i.e., open-loop poles at $z = 1.0$. For stability, we want these poles to move inside the unit circle with increasing G. The closer the zeros are to the point $z = 1.0$, the faster the poles at $z = 1.0$ will move inside the unit circle. Since here all gains and loop parameters are controlled digitally, there is no danger of instabilities due to drifts of gain values as is the case with analog loops. However, it should be checked that any quantization and truncation errors will not produce undesirable fluctuations in the locations of z_i and p_i.

Performing a root-locus analysis and simulation revealed that the range of allowable G values increases when the poles are forced to stay longer on the real axis. A rule of control theory states that the root locus on the real axis always lies in a section of this axis to the *left* of an *odd* number of poles and zeros. Figure 5 illustrates some root locus diagrams with the number of integrators, N, in $F(z)$ being a parameter.

Using this simple rule, the minimum number of zeros near $z = 1.0$ was determined. For each pole of $F(z)$ at $z = 1.0$, one zero is required. These $m = N$ zeros will force the poles at $z = 1.0$ to move inside the unit circle as shown in Fig. 5. Note from Eq. (8) that the system transfer function contributes one pole at $z = 1.0$. Thus, the total number of poles at $z = 1.0$ (integrators) is $N + 1$.

By trial and error, it was found that, with any number of integrators, the gain margin increases when the open loop transfer function, $G(z)$ has a minimum number of poles. Since the transfer function contributes two poles at $z = 0$ (see Eq. [8]), which try to move quite fast out of the unit circle when the loop gain is increased, it is desirable to cancel these two poles with two zeros at the origin. From Eq. (16), this implies that $n - m = 2$. Since, from the above, the number m of zeros not at the origin was selected equal to the number N of integrators, then the *total* number of poles of $F(z)$ is given by

$$n = m + 2 = N + 2 \quad (18a)$$

and $F(z)$ will be of the form

$$F(z) = \frac{(z - z_1)(z - z_2) \ldots (z - z_N) z^2}{(z - p_1)(z - p_2)(z - 1)^N} \qquad (18b)$$

Finally, using Eq. (18b) in Eq. (8) results in an open loop transfer function of the desired form, namely

$$G(z) = G \frac{(z - z_a)(z - z_b)(z - z_1)(z - z_2) \ldots (z - z_N)}{(z - p_1)(z - p_2)(z - 1)^{N+1}} \qquad (18c)$$

The order of $G(z)$ will be $N + 3$, and the degree of its numerator will be one less than that of the denominator.

The lower bound on the allowable gain G is determined by the proximity of z_i to the point $z = 1.0$. The upper bound on G is controlled by the location of the poles p_1 and p_2 since as G increases these poles move outside the unit circle. By trial and error, it was found that the poles originating at p_1 and p_2 will stay longer inside the unit circle when p_1 and p_2 are placed on the real axis between $z = -1.0$ and $z = z_a$. The maximum upper bound on G is achieved when p_1 is very close to $z = -1.0$ and p_2 is very close to $z = z_a$. The root locus of these two poles is shown in Fig. 5.

Figure 6 illustrates the impact of the location of z_1 on the loop gain margin for the case when $N = 1$.

B. Noise-Equivalent Bandwidth

The closed loop transfer function $H(z)$ of Eq. (17) can be rewritten as

$$H(z) = \frac{B(z)}{A(z)} = \frac{b_0 z^{n+1} + b_1 z^n + \ldots + b_{n+1}}{a_0 z^{n+1} + a_1 z^n + \ldots + a_{n+1}} \qquad (19)$$

(Our loop has $b_0 = 0, a_0 = 1$.)

The one-sided noise-equivalent bandwidth is defined as

$$B_L = \frac{1}{2TH^2(1)} \frac{1}{2\pi j} \oint H(z) H(z^{-1}) \frac{dz}{z} \qquad (20)$$

$$= \frac{1}{2TH^2(1)} I_n \qquad (21)$$

Let

$$\Omega = \begin{bmatrix} a_0 & a_1 & a_2 & \ldots & a_{n+1} \\ a_1 & a_0 + a_2 & a_1 + a_3 & \ldots & a_n \\ a_2 & & & & \\ \cdot & & & & \\ \cdot & & & & \\ \cdot & & & & \\ a_{n+1} & 0 & 0 & \ldots & a_0 \end{bmatrix} \qquad (22)$$

and Ω_1 be the matrix formed from Ω by replacing the first column of Eq. (22) with

$$\begin{bmatrix} \sum_{i=0}^{n+1} b_i^2 \\ 2 \sum_{i=0}^{n+1} b_i b_{i+1} \\ 2 \sum_{i=0}^{n+1} b_i b_{i+2} \\ \cdot \\ \cdot \\ \cdot \\ 2 b_0 b_{n+1} \end{bmatrix} \qquad (23)$$

According to Ref. 2, the integral I_n is equivalent to the ratio of two determinants as follows:

$$I_n = \frac{|\Omega_1|}{a_0 |\Omega|} \qquad (24)$$

Using Eqs. (22), (23) and (24) in Eq. (21), the bandwidth vs G was calculated for the filters and gain values given in Table 1, and plotted in Figs. 7-11. For loops which are similar in their pole-zero location, increasing the number of integrators in $F(z)$ increases B_L. Adding more poles and/or zeros near $z = 0$ has an insignificant impact on the bandwidth. The impact of the location of z_1 on the bandwidth when $N = 1$ is shown in Fig. 6. B_L was computed for $G = G_{min} + 4$ dB.

C. Steady-State Error

The input to our z-domain loop (see Fig. 2) can be expressed as

$$\left(\frac{\theta(s)}{s}\right)^* = \frac{\theta_1 T z}{(z-1)^2} + \frac{\theta_2 T^2 z(z+1)}{2(z-1)^3} + \frac{\theta_3 T^3 z(z^2+4z+1)}{3(z-1)^4} + \frac{\theta_4 T^4 z(z^3+11z^2+11z+1)}{4(z-1)^5} + \ldots \quad (25)$$

where θ_1, θ_2, θ_3, θ_4 represent phase step, ramp, acceleration and jerk, respectively. Higher orders terms are assumed to be negligible.

The transfer function $H_\epsilon(z)$ is defined as

$$H_\epsilon(z) = \frac{\epsilon(z)}{\left(\frac{\theta(s)}{s}\right)^*} = \frac{G_Q(z-1)}{z(1+G(z))} \quad (26)$$

where $G(z)$ is given by Eq. (8) which results in the steady state error

$$\epsilon_{ss} = \lim_{z\to 1} \left(\frac{z-1}{z}\right) H_\epsilon(z) \left(\frac{\theta(s)}{s}\right)^* \quad (27)$$

Let $F(z)$ be of the form in Eq. (18b). Then, inserting Eqs. (25) and (26) in Eq. (27) and simplifying, we obtain

$$\epsilon_{ss} = \lim_{z\to 1} \left[\frac{\theta_1 T z}{(z-1)^2} + \frac{\theta_2 T^2 z(z+1)}{2(z-1)^3} + \frac{\theta_3 T^3 z(z^2+4z+1)}{3(z-1)^4} + \frac{\theta_4 T^4 z(z^3+11z^2+11z+1)}{4(z-1)^5}\right] \times \frac{G_Q(z-p_1)(z-p_2)(z-1)^{N+3}}{z^2[(z-1)^{N+1}(z-p_1)(z-p_2) \ldots + G(z-z_a)(z-z_b)(z-z_1)\ldots(z-z_N)]} \quad (28)$$

With $N = 1$, θ_3 (phase acceleration) will be tracked with finite steady-state error, but θ_4 (phase jerk) will generate infinite steady-state error. With $N = 2$, θ_4 will be tracked with finite steady-state error. With $N \geq 3$ the steady-state error due to phase jerk will be zero. Table 2 lists values of steady-state error for different values of N. Note that the proximity of z_i to the point $z = 1.0$ increases the value of the steady-state error.

Steady-state *phase error*, ϕ_{ss}, can be readily obtained from ϵ_{ss}, using the relation

$$\phi_{ss} = \frac{\epsilon_{ss}}{G_Q T} \quad (29)$$

which is equivalent to

$$\phi_{ss} = \frac{\epsilon_{ss} T(1-g)^2}{2G} \quad (30)$$

by using Eq. (9).

D. Transient Response

In general, for a digital loop with a large number of poles and zeros, it is not easy to calculate the transient response. If, for some specific gain value, the loop has only two dominant poles, then the natural frequency, damping ratio and settling time can be assessed from the second-order loop equations. Otherwise, an inverse z-transform operation has to be performed on the product of the loop transfer function and the step input. There are three methods available for this inverse z-transformation: integration, partial fraction expansion and long division. In our analysis, we have chosen the last of the three.

By performing synthetic (long) division on the ratio of two polynomials in

$$\epsilon(z) = \frac{G_Q(z-1)}{z(1+G(z))} \times \frac{\theta_1 T z}{(z-1)^2} = \epsilon_1 z^{-1} + \epsilon_2 z^{-2} + \epsilon_3 z^{-3} + \ldots \quad (31)$$

the time response of the loop with a step input is obtained at time t_1, t_2, t_3, etc. The settling time T_s is determined when the magnitudes of ϵ_i become less than, say, 5% of the initial value for all t_i, t_{i+1}, etc. Plots of T_s vs G for a loop with filters specified in Table 1 are shown in Figs. 7-11. As can be seen from these figures, the settling time increases very sharply when the two poles on the left portion of the real axis migrate close to the unit circle (see Fig. 5). The impact of the location of z_1 on T_s for $N = 1$ is shown in Fig. 6.

IV. Conclusion

In this article, a model for a general digital-phase locked loop is proposed. The impact of a digital filter on the stability, gain margin, noise-equivalent bandwidth and time response is investigated. A specific type of digital filter is proposed which, for any desired number of integrators, has a minimum number of zeros. The strategy adopted in this analysis in optimizing

the loop performance with the digital filter consists of two steps. First, the lower and upper bounds of the allowable loop gain are obtained by placing the filter's zeros close to the point $z = 1.0$ and the two filter's poles close to $z = -1.0$ and $z = z_a$. Then, the desired bandwidth and settling time are obtained by selecting the corresponding value for the loop gain.

Table 2 lists steady-state error values vs the number of integrators of the loop filter. Making the number of integrators equal to 3, the loop can track phase jerk with zero steady-state error (at loop update instants). Figures 7 through 11 show the variation of the noise bandwidth and settling time with changing gain for different loop types.

References

1. Winkelstein, R. A., "Analysis of the Signal Combiner for Multiple Antenna Arraying," *Deep Space Network Progress Report 42-26*, January and February 1975, pp. 102-118, Jet Propulsion Laboratory, Pasadena, California.

2. Jury, E. I., *Theory and Applications of the Z-Transform Method*, R. E. Krieger, Florida, 1982.

Table 1. Proposed placement of poles and zeros for loop filters

Location of Poles and Zeros[1] of $F(z)$	Number of Integrators of $F(z)$				
	0	1	2	3	4
z_1		0.960	0.960	0.960	0.970
z_2			0.960	0.930	0.960
z_3				0.930	0.940
z_4					0.940
p_1	−0.173	−0.173	−0.173	−0.173	−0.173
p_2	−0.999	−0.999	−0.999	−0.999	−0.999
p_3		1.000	1.000	1.000	1.000
p_4			1.000	1.000	1.000
p_5				1.000	1.000
p_6					1.000
Approximate range of G	0.001 0.30	0.001 0.30	0.01 0.30	0.04 0.30	0.04 0.30

[1] $F(z)$ contains also $n - m$ zeroes at $z = 0$. In our analysis $n - m = 2$.

Table 2. Steady-state error signal vs loop type

Loop Type	Steady State Error, e_{ss}		
	Phase Ramp	Phase Acceleration	Phase Jerk
1	$\theta_2(1-p_1)(1-p_2)$	∞	∞
2	0	$\dfrac{2\theta_3 T(1-p_1)(1-p_2)}{(1-z_1)}$	∞
3	0	0	$\dfrac{6\theta_4 T^2(1-p_1)(1-p_2)}{(1-z_1)(1-z_2)}$
4	0	0	0

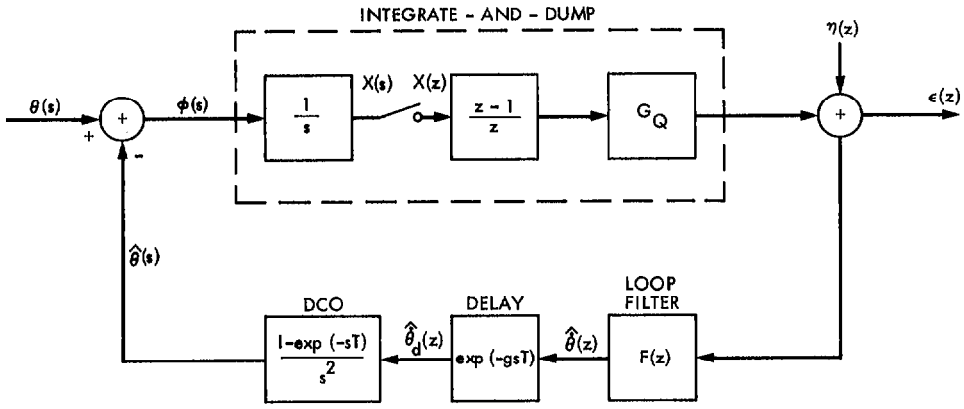

Fig. 1. Closed loop hybrid *s/z* diagram

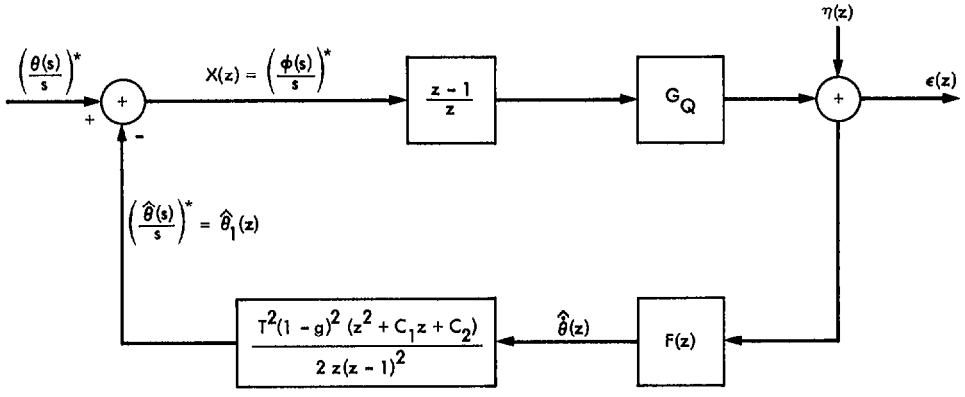

Fig. 2. Equivalent closed loop z-domain diagram

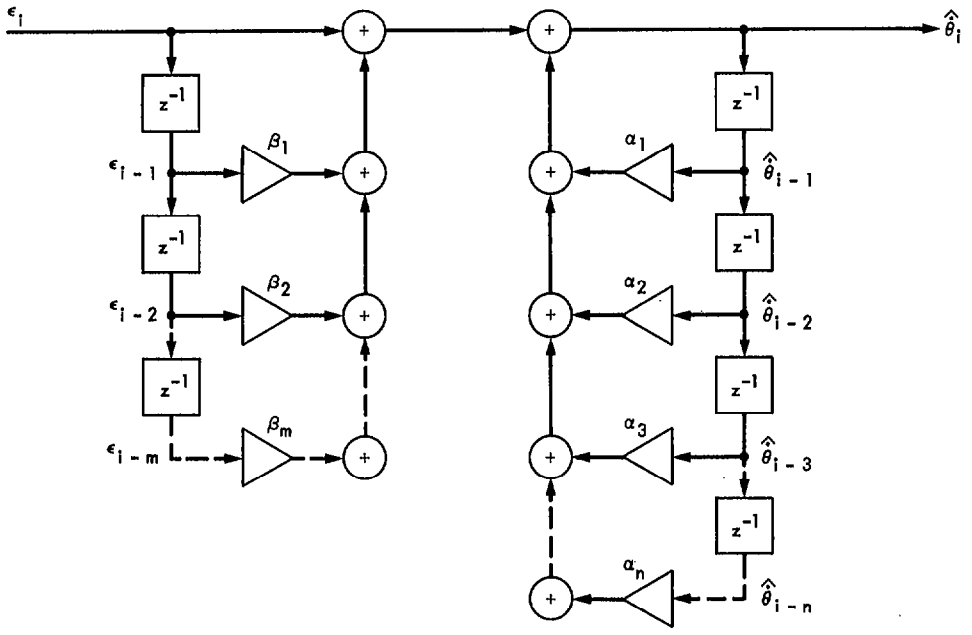

Fig. 3. Direct form I realization of $F(z)$

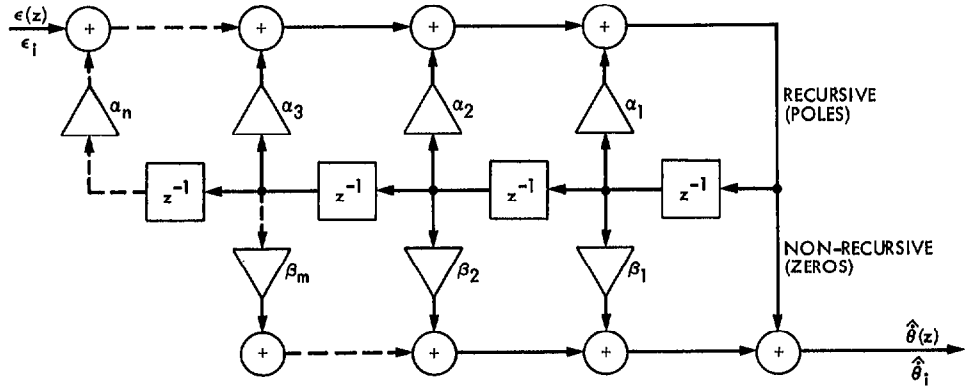

Fig. 4. Direct form II realization of $F(z)$

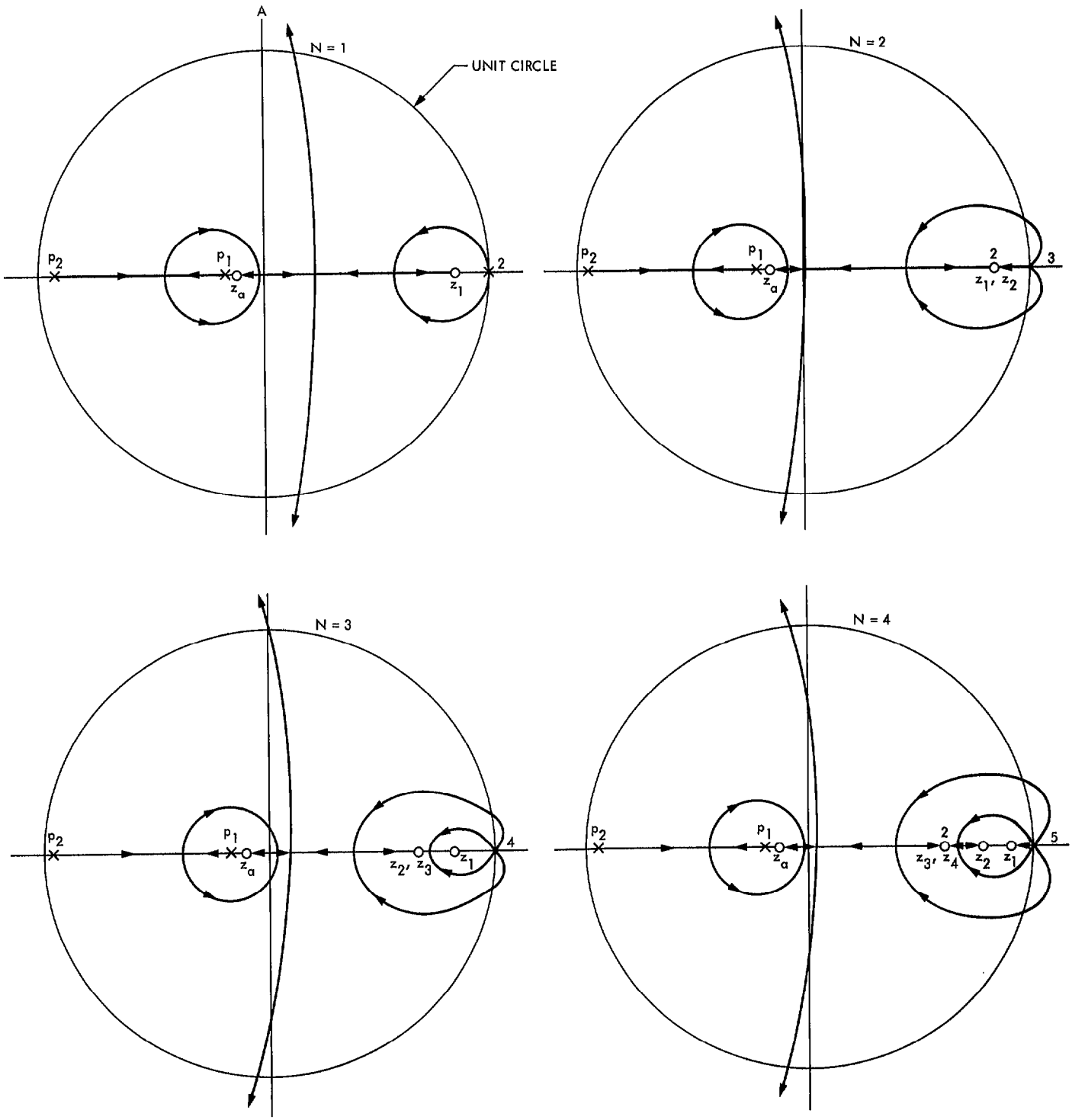

Fig. 5. Root-locus in the complex z-plane. *N* = number of integrators of *F*(z).

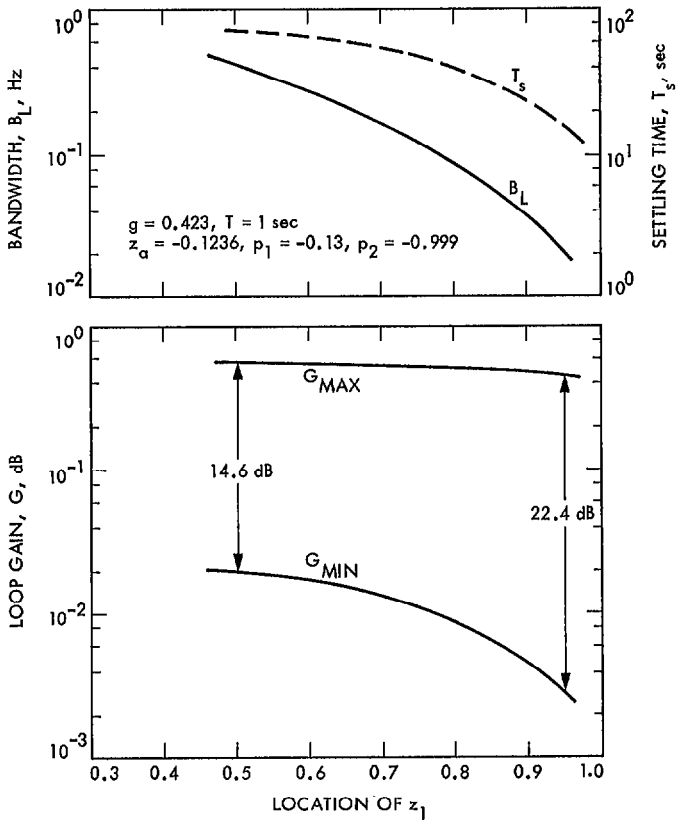

Fig. 6. G_{max}, G_{min}, B_L and T_S vs location of z_1, for $F(z)$ with 1 integrator

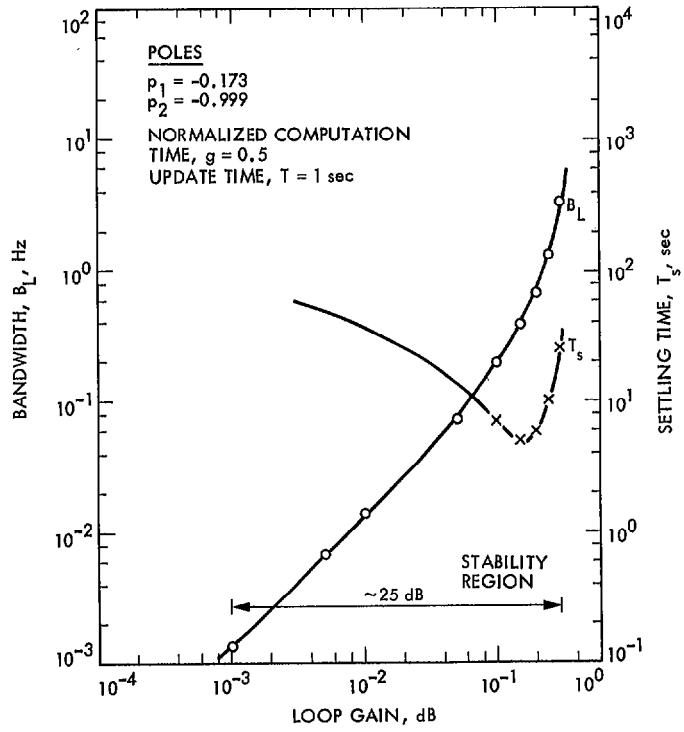

Fig. 7. Bandwidth and settling time vs loop gain. Number of integrators: 0.

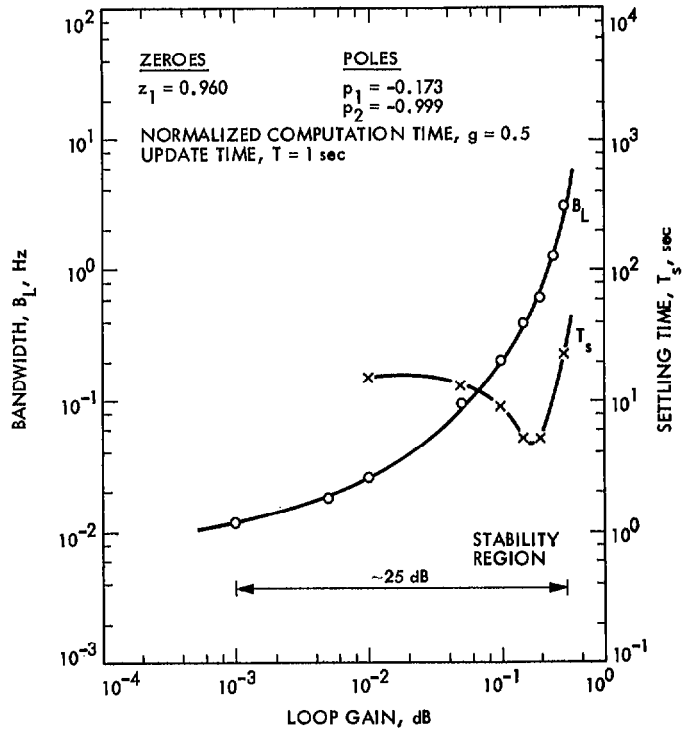

Fig. 8. Bandwidth and settling time vs loop gain. Number of integrators: 1.

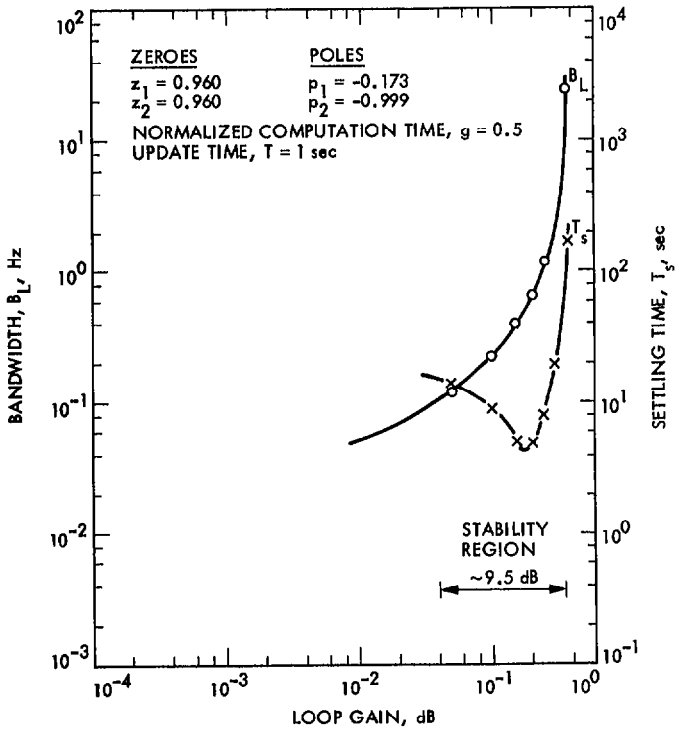

Fig. 9. Bandwidth and settling time vs loop gain. Number of integrators: 2.

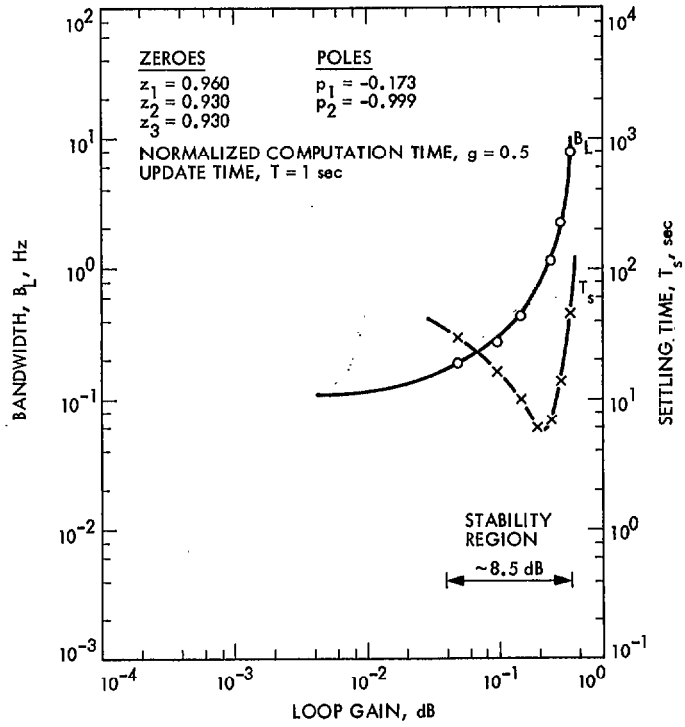

Fig. 10. Bandwidth and settling time vs loop gain. Number of integrators: 3.

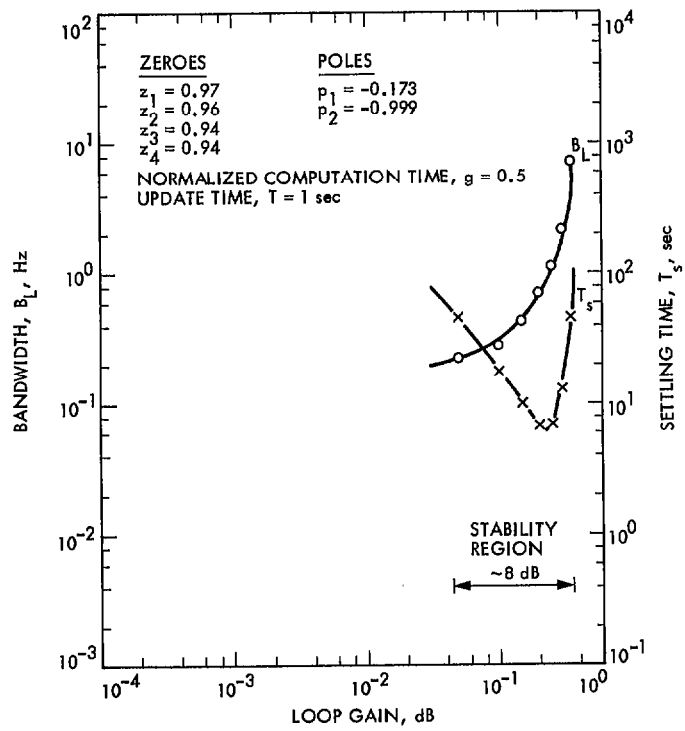

Fig. 11. Bandwidth and settling time vs loop gain. Number of integrators: 4.